LOW COST MINIATURIZED EHF SATCOM TRANSCEIVER FEATURING HEMT MMICS AND LTCC MULTILAYER PACKAGING

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ABSTRACT

Presented is a 20 GHz downconverter and a 44 GHz upconverter for a low cost miniaturized transceiver for EHF SATCOM terminal applications. The hardware features a set of passivated pseudomorphic InGaAs HEMT MMICs including a 20 GHz balanced low noise amplifier and a 44 GHz 100 mW driver amplifier. The upconverter input and the LO input of the downconverter feature built-in-test (BIT) with on-chip detectors. The downconverter is packaged in a low temperature co-fired ceramic (LTCC) substrate, with integrated RF and DC interconnects, printed resistors, and a buried stripline IF filter.

INTRODUCTION

The performance and cost drivers of the transceiver for future EHF SATCOM terminals include low noise figure, high reliability, small size and weight, and low power consumption [1]. HEMT MMIC technology has been demonstrated as a viable solution to meet both the low cost and high performance requirements for these applications. We have previously reported on a set of five high performance HEMT MMIC chips that provides the necessary RF functions for an EHF SATCOM transceiver system [2]. Further miniaturization and cost reduction of these EHF SATCOM terminals relies on the successful insertion of these multifunction MMICs into small, low-cost, highly integrated packages. We have used multilayer ceramic packaging technology to build the 20 GHz downconverter subsystem (Figure 1) with integrated RF and DC interconnects, printed thick-film resistors, and a buried stripline IF filter. The upconverter has been packaged using carrierless microwave

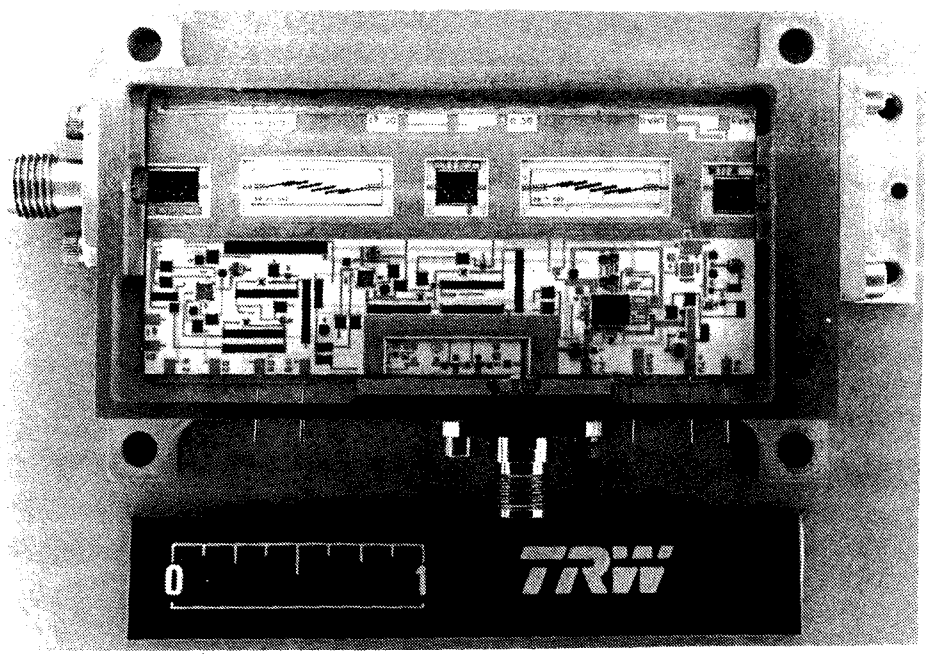

Figure 1. K-Band Downconverter Assembly Using LTCC Multilayer Substrate.

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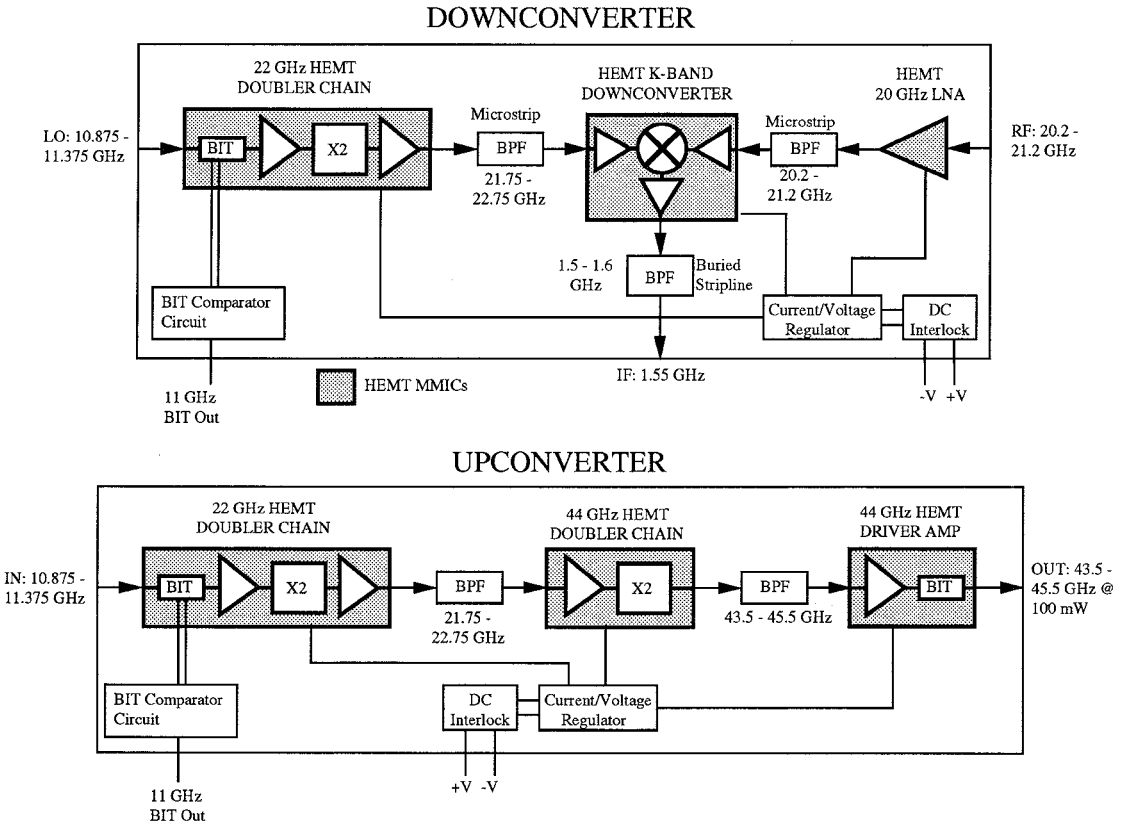


Figure 2. Downconverter and Upconverter System Block Diagrams.

assembly techniques and is very compact. Both the upconverter and downconverter feature a DC interlock circuit to ensure the MMICs receive negative gate bias before the positive drain bias. Both units feature voltage and current regulation from a monolithic silicon regulator chip.

TRANSCEIVER SYSTEM

Figure 2 show block diagrams of the downconverter and upconverter subsystems. The downconverter consists of the 20 GHz LNA, an image reject filter, the K-Band downconverter MMIC, the 22 GHz doubler chain with filter for the LO, and the buried 1.55 GHz IF filter. The 11 GHz LO input signal is monitored through the BIT detection circuit integrated on the 22 GHz doubler chain MMIC. The three MMICs are regulated by a monolithic voltage/current regulator and the DC interlock circuitry protects the MMICs with voltage sequencing.

The upconverter/transmitter features the same 22 GHz doubler chain and bandpass filter as the downconverter, the 44 GHz doubler chain, another bandpass filter, and the 44 GHz driver amplifier that puts out better than 100 mW of output power. These three MMICs are regulated by a monolithic voltage/current regulator and protected by DC interlock circuitry.

HEMT MMIC CIRCUITS

The five MMICs used in these subsytems were previously presented in reference [2]. They were all fabricated using TRW's 0.15 μm planar-doped pseudomorphic InGaAs T-gate HEMT process with SiN passivation. The 20 GHz balanced LNA has a noise figure of 1.8 dB, an associated gain of 31 dB, and better than 1.3:1 VSWR over the 20.1-21.2 GHz band. The 20 GHz downconverter MMIC has 15 dB of conversion gain and less than 6 dB of noise figure.

The 22 GHz doubler chain is a multifunction chip that includes an input BIT detector, 2 stages of amplification and a frequency doubler. The circuit is used in both the upconverter and downconverter units. This doubler chain delivers +10 dBm of output power from 21.75 to 22.75 GHz with 14 dB of

conversion gain. The 44 GHz doubler chain delivers +9 dBm or more of output power from 43 to 46 GHz with 4 dB of conversion gain. The 3-stage 44 GHz driver amplifer has 18 dB of small signal gain and delivers +21.7 dBm (150 mW) of output power at a drain bias of +5 volts. For this application, the amplifier was only biased +3.5 volts, however.

LTCC DOWNCONVERTER PACKAGE

The completed downconverter is shown in Figure1. The MMIC chips and all DC circuitry are mounted on the LTCC substrate. The LTCC is composed of 9 layers of DuPont 851 fired ceramic, fabricated by CTS Corporation. The LTCC is mounted in an Al-Si housing and has a WR-28 waveguide input for the RF and SMA connectors for the LO input and IF output. The RF input is transitioned from waveguide to microstrip by means of an E-plane probe.

Figure 3 shows a cross-section of the LTCC tape stack-up, indicating that the bottom 6 layers are used to create a stripline environment for RF interconnect and for the buried 1.55 GHz bandpass filter. Each layer of the structure is a post-fired 3.7 mils thick. The 4 mil thick MMICs are mounted on the second layer of the tape structure, providing a good height match to the RF interconnect layer. Below each chip mounting cavity are a series of ground vias for providing good RF, DC, and thermal paths. The top 3 layers of the LTCC are used for DC routing; connecting the interlock, regulator, and BIT functions together with the MMICs. Vertical vias are used in cross-over points and for passing the MMIC biasing voltages down to the RF interconnect layer, where they emerge into the cavity for connection to the MMICs. Thick film resistors using multiple decade sheet resistance materials are deposited on the top layer of the tape stack-up.

The measured performance of the downconverter is shown in Figure 4. The noise figure is measured at the waveguide flange to be below 2.4 dB with an associated gain of about 36 dB.

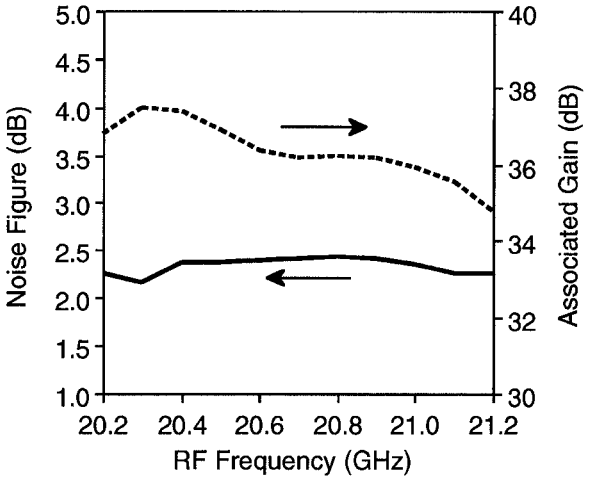


Figure 4. Measured Downconverter NF and Gain.

UPCONVERTER IMA PACKAGE

The upconverter shown in Figure 5 is packaged using traditional integrated microwave assembly (IMA) packaging techniques. The RF chain is assembled in a channelized housing made of an aluminum-silicon alloy. The DC circuitry is assembled in a separate cavity in the housing, with small channels connecting into the RF cavity. The 11 GHz input to the unit is provided by an SMA connector and the output goes to WR-22 waveguide through an E-plane probe transition.

The measured output power compression is shown in Figure 6 at the center frequency of 44.5 GHz. The desired input power to the

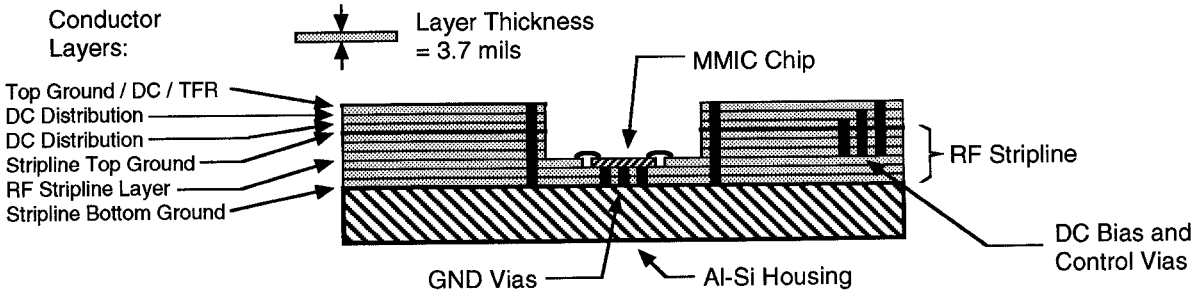


Figure 3. LTCC Layer Stack-Up for Downconverter Assembly.

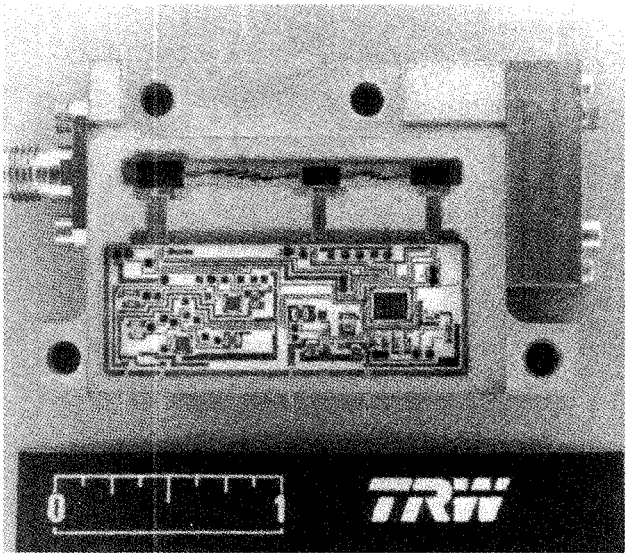
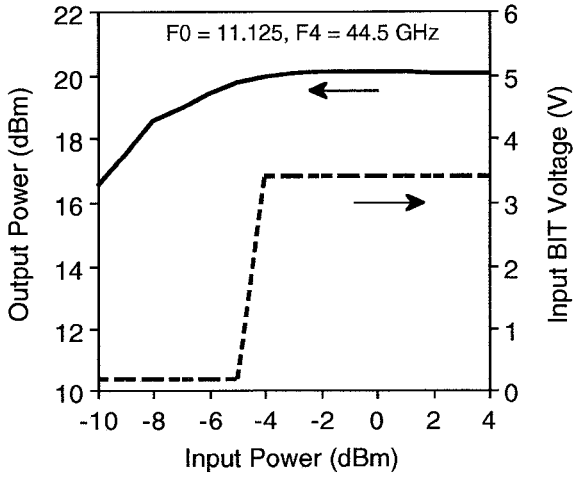


Figure 5. Q-Band Upconverter IMA Package.

upconverter is -4 dBm so the input BIT detector on the 22 GHz doubler chain is set to trigger if the input power falls below that level. While the input power remains above -4 dBm, the BIT detector output voltage remains high, as shown in Figure 6. The measured output power and input return loss versus output frequency are shown in Figure 7 at an input power of -4 dBm. The output power peaks at +20 dBm (100 mW) and is greater than +17.8 dBm across the band. The input return loss is below -22.5 dB across the band.



ure 6. Pout Compression and BIT Voltage.

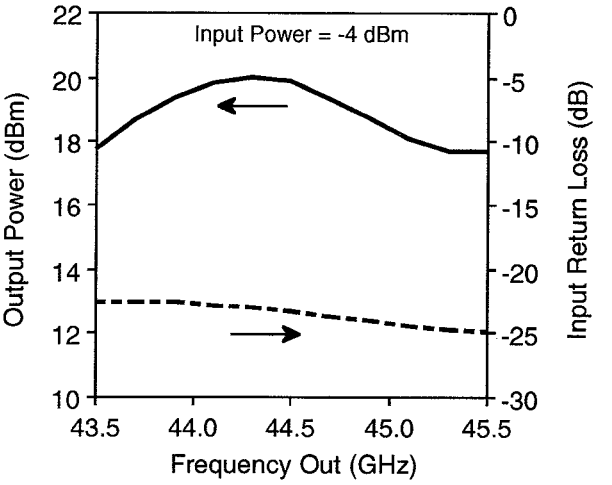


Figure 7. Output Power and Input Return Loss.

CONCLUSION

We have developed a high performance 20 GHz downconverter for EHF SATCOM transceiver applications using an LTCC multilayer ceramic packaging technique, leading the way to lower cost units for large volume production. We have also developed a small integrated 44 GHz upconverter for transmitter applications. Both units are highly compact, yet have a high degree of functionality for stand alone operation, featuring DC interlock circuitry, voltage and current regulation, and BIT detection.

ACKNOWLEDGEMENTS

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